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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,582	10/12/2005	Shinsuke Harada	270968US2X PCT	1837

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EXAMINER	
KIM, JAY C	
ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/531,582	HARADA ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-22 and 27* is/are pending in the application.

4a) Of the above claim(s) *18,19 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-17,20,21 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/21/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to RCE filed October 25, 2010.

Claim Objections

1. Claims 14 and 27 are objected to because of the following informalities:

On line 5 of claim 14, newly added “impurity” should be removed.

On line 7 of claim 27, “impurity” should be inserted between “high” and “concentration”.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what Applicants claim by “high concentration gate regions including the high impurity concentration gate region of the second conductivity type are respectively directly deposited on surfaces of the high impurity concentration gate regions of the second conductivity type" on lines 7-9, because Applicants claim that high impurity concentration gate regions are deposited onto themselves.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 13, 15, 17 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueno (JP 05-259443).

Regarding claim 13, Ueno discloses a silicon carbide semiconductor device (Fig. 1 and [0001]) comprising a lower deposition film (layer 4 below the broken line, also in Fig. 2(a)) which is formed of a single layer of silicon carbide of a first conductivity type (n-type), and which has lower impurity concentration (n^-) than a high impurity concentration (n^+) silicon carbide substrate (5) of the first conductivity type and which is formed on a surface of the silicon carbide substrate, a high impurity concentration gate region (9) of a second conductivity type (p-type) selectively formed across from an upper surface to an interior of the lower deposition film, the high impurity concentration gate region being adjacent to and in contact with a non-implanted portion (portion of layer 4 directly under the broken line) that is an exposed part of the upper surface of the lower deposition film (4), an upper deposition film (3 in Figs. 1 and 2(b)) formed on the lower deposition film in which the high impurity concentration gate region (9) is formed, wherein the upper deposition film comprises a low impurity concentration gate region (8) of the second conductivity type (p-type) directly deposited on a surface of the high impurity concentration gate region (9) of the second conductivity type and having a

lower impurity concentration (p) than the high impurity concentration (p^+) gate region, a high impurity concentration source region (6) of the first conductivity type (n-type) selectively formed on part of an upper surface of the low impurity concentration gate region of the second conductivity type and being more heavily doped (n^+) than the low impurity concentration gate region (8, p) of the second conductivity type (p-type), and a low impurity concentration base region (n^- region directly above the broken line) of the first conductivity type (n-type) formed on the non-implanted portion and having a greater width than the non-implanted portion (n^- region directly under the broken line) and being doped less (n^-) than the high impurity concentration (n^+) source region (6) of the first conductivity type, a gate insulation film (2) formed on at least a surface of the upper deposition film (3), a gate electrode (1) formed via the gate insulation film, a drain electrode (12) having a low-resistance contact connection with a backside of the silicon carbide substrate (5) of the first conductivity type (n-type), and a source electrode (10) having a low-resistance contact connection with part of the high impurity concentration source region (6) of the first conductivity type and the low impurity concentration gate region (8) of the second conductivity type (p-type) via a highly doped p^+ region 7.

Regarding claims 15 and 17, Ueno further discloses that the low impurity concentration base region (n^- region directly above the broken line) of the first conductivity type (n-type) has a lower impurity concentration than the high impurity concentration gate region (9) of the second conductivity type (p-type) (claim 15), wherein the upper deposition film (3) is constituted of silicon carbide (claim 17).

Regarding claim 27, Ueno further discloses for the silicon carbide semiconductor device according to claim 13 that high impurity concentration gate regions (9) including the high impurity concentration gate region (9) of the second conductivity type (p-type) are formed on both sides of the non-implanted portion (n^- region directly under the broken line) so that the non-implanted portion will be formed in an intermediate part of the upper surface of the lower deposition film (4), high impurity concentration gate regions (9) including the high impurity concentration gate region (9) of the second conductivity type (p-type) are respectively directly deposited on surfaces of the high impurity concentration gate regions (9) of the second conductivity type (p-type) on both sides of the base region (n^- region directly above the broken line) of the first conductivity type (n-type), and source regions (6 in Figs. 1 and 2(d)) including the source region (6) of the first conductivity type are respectively formed on parts of upper surfaces of the low impurity concentration gate regions (8) of the second conductivity type on both sides of the base region of the first conductivity type.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (JP 05-259443). The teachings of Ueno are discussed above.

Regarding claims 14 and 16, Ueno further discloses for the silicon carbide semiconductor device according to claim 13 that the low impurity concentration gate region (8) of the second conductivity type (p-type) selectively formed in the upper deposition film (3) has a portion that is in contact with the gate insulation film (2).

Ueno differs from the claimed invention by not showing that the upper deposition film has a thickness within a range of 0.2 μm to 0.7 μm and the low impurity concentration gate region has an impurity concentration higher than 1×10^{15} cm^{-3} and lower than 5×10^{15} cm^{-3}. (claim 14), and has an impurity concentration of not higher than 2×10^{16} cm^{-3} (claim 16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the silicon carbide semiconductor device disclosed by Ueno may comprise an upper deposition film thickness and a low concentration gate region impurity concentration within the claimed ranges, because the upper deposition film thickness and the low concentration gate region impurity concentration can be controlled to achieve desired silicon carbide semiconductor device characteristics to improve performance of the silicon carbide semiconductor device. Further, the claims are *prima facie* obvious without showing that the claimed ranges of the thickness and impurity concentration achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of

the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

8. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (JP 05-259443) in view of Okuno et al. (US 6,165,822). The teachings of Ueno are discussed above.

Regarding claims 20 and 21, Ueno differs from the claimed invention by not showing that in terms of crystal Miller index the surface of the silicon carbide substrate of the first conductivity type is a plane that is parallel to a (11-20) plane (claim 20) or a plane that is parallel to a (000-1) plane (claim 21).

Okuno et al. disclose a silicon carbide semiconductor device (Fig. 7C), wherein in terms of crystal Miller index a surface (top or bottom surface) of a silicon carbide substrate (1) of the first conductivity type (n-type) is a plane that is parallel to a (11-20) plane or a plane that is parallel to a (000-1) plane (col. 5, lines 10-14).

Since both Ueno and Okuno et al. teach a silicon carbide semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the silicon carbide substrate disclosed by Ueno may have a surface parallel to a (11-20) or (000-1) plane as disclosed by Okuno et al., because those two planes are well-known silicon carbide surface planes to form a silicon carbide semiconductor device due to their well-known physical and electrical characteristics.

Response to Arguments

9. Applicants' arguments with respect to claim 13 have been considered but are moot in view of the new ground of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
February 11, 2011

/Jay C Kim/
Examiner, Art Unit 2815